

PRODUCT SPECIFICATION

FLXF-BL3296-40D(I)

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10Gb/s Tx1330/Rx1270nm XFP 40Km

10Gb/s Tx1270/Rx1330nm XFP 40Km

■ Features:

- ★ Supports 9.95Gb/s to 11.3Gb/s bit rates
- ★ Hot Pluggable XFP Footprint
- ★ 1330/1270nm DFB Laser and PIN photo detector
- ★ Up to 40km transmission on SMF
- ★ Power dissipation < 2W
- ★ Single Power Supply: 3.3V
- ★ No Reference Clock Required
- ★ Compatible with RoHS
- ★ Built-in Digital Diagnostic Functions



■ Applications:

- ★ 10GBASE-LR/LW 10G Ethernet
- ★ SONET OC-192 SR-1
- ★ SDH STM I-64.1
- ★ 1200-SM-LL-L 10G Fibre Channel
- ★ 10GBASE-LR/LW with FEC
- ★ 1200-SM-LL-L 10G Fibre Channel with FEC

■ Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Storage Temperature	Tst	-40	+85	°C
Supply Voltage	Vcc	0	+3.6	V
Operating Relative Humidity	RH	0	85	%

■ Operation Environment

Parameter	Symbol	Min	Typical	Max	Units
Supply Voltage	V _{cc}	3.15		3.45	V
Operating Case Temperature	T _c	0		+70	°C
Power Dissipation				2	W
Data Rate		9.95		11.3	Gbps

■ Optical Characteristics

(Ambient Operating Temperature 0°C to +70°C, V_{cc} =3.3 V)

Parameter		Symbol	Min.	Typ.	Max.	Units
Transmitter Section						
Center Wavelength	Tx 1270	λ_o	1250	1270	1290	nm
	Tx 1330		1310	1330	1350	
Spectral Width(-20dB)	Tx 1270	$\Delta\lambda$			1	nm
	Tx 1330				1	
Average Output Power	Tx 1270	P_o	0		+5	dBm
	Tx 1330		0		+4	
Extinction Ratio		E_r	3.5			dB
Side-Mode Suppression Ratio		SMSR	35			dB
Total jitter		T_j	IEEE 802.3ae			
Receiver Section						
Center Wavelength	Rx 1330	λ_o	1310	1330	1350	nm
	Rx 1270		1250	1270	1290	
Receiver Sensitivity		R_{sen}			-15	dBm
Receiver Overload		R_{ov}	-3			dBm
Return Loss			12			dB
LOS Assert		LOS_A	-30			dBm
LOS Dessert		LOS_D			-18	dBm
LOS Hysteresis			0.5		4	

Electrical Characteristics

(Ambient Operating Temperature 0°C to +70°C, Vcc =3.3 V)

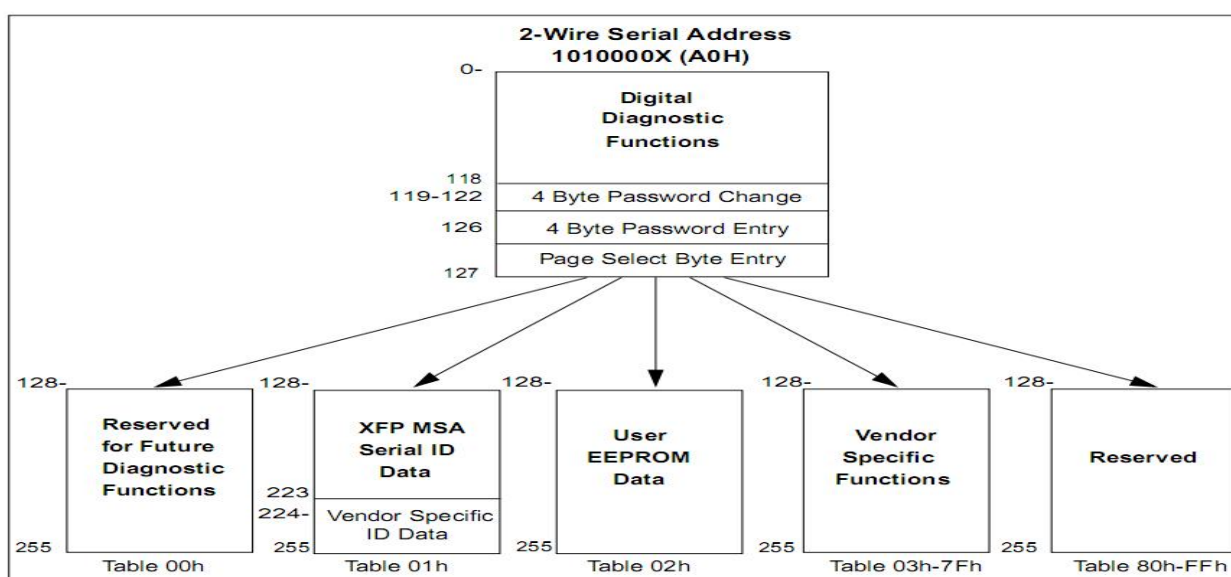
Parameter		Symbol	Min.	Typ.	Max.	unit
Transmitter Section						
Input Differential Impedence		Zin	90	100	110	Ohm
Data Input Swing Differential		Vin	120		850	mV
TX Disable	Disable		2.0		Vcc	V
	Enable		0		0.8	V
TX Fault	Assert		2.0		Vcc	V
	Deassert		0		0.8	V
Receiver Section						
Output differential impedance		Zout		100		Ohm
Data output Swing Differential		Vout	340	650	850	mV
Rx_LOS	Assert		2.0		Vcc	V
	Deassert		0		0.8	V

Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	-10 ~ 75	±3	°C	Internal
Bias Current	0 ~ 100	0.5	mA	Internal
Tx Power	-5 ~ +5	±1	dBm	Internal
Rx Power	-18 ~ 0	±1	dBm	Internal

For more detailed information including memory map, please see XFP MSA Specification

EEPROM INFORMATION (A0) :



■ Pin Description:

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Module Ground	1
2		VEE5	Optional -5.2 Power Supply – Not required	
3	LVTTL-I	Mod-Desel	Module De-select; When held low allows the module to respond to 2-wire serial interface commands	
4	LVTTL-O	Interrupt	Interrupt (bar); Indicates presence of an important condition which can be read over the serial 2-wire interface	2
5	LVTTL-I	TX_DIS	Transmitter Disable; Transmitter laser source turned off	
6		VCC5	+5 Power Supply– Not required	
7		GND	Module Ground	1
8		VCC3	+3.3V Power Supply	
9		VCC3	+3.3V Power Supply	
10	LVTTL-I	SCL	Serial 2-wire interface clock	2
11	LVTTL-I/O	SDA	Serial 2-wire interface data line	2
12	LVTTL-O	Mod_Abs	Module Absent; Indicates module is not present. Grounded in the module.	2
13	LVTTL-O	Mod_NR	Module Not Ready; Finisar defines it as a logical OR between RX_LOS and Loss of Lock in TX/RX.	2
14	LVTTL-O	RX_LOS	Receiver Loss of Signal indicator	2
15		GND	Module Ground	1
16		GND	Module Ground	1
17	CML-O	RD-	Receiver inverted data output	
18	CML-O	RD+	Receiver non-inverted data output	
19		GND	Module Ground	1
20		VCC2	+1.8V Power Supply – Not required	
21	LVTTL-I	P_Down/RST	Power Down; When high, places the module in the low power stand-by mode and on the falling edge of P_Down initiates a module reset Reset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.	
22		VCC2	+1.8V Power Supply – Not required	
23		GND	Module Ground	1
24	PECL-I	RefCLK+	Reference Clock non-inverted input, AC coupled on the host board – Not required	3
25	PECL-I	RefCLK-	Reference Clock inverted input, AC coupled on the host board – Not required	3
26		GND	Module Ground	1
27		GND	Module Ground	1
28	CML-I	TD-	Transmitter inverted data input	
29	CML-I	TD+	Transmitter non-inverted data input	
30		GND	Module Ground	1

Notes:

1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector; should be pulled up with 4.7k – 10kohms on host board to a voltage between 3.15V and 3.6V
3. A Reference Clock input is not required. If present, it will be ignored.

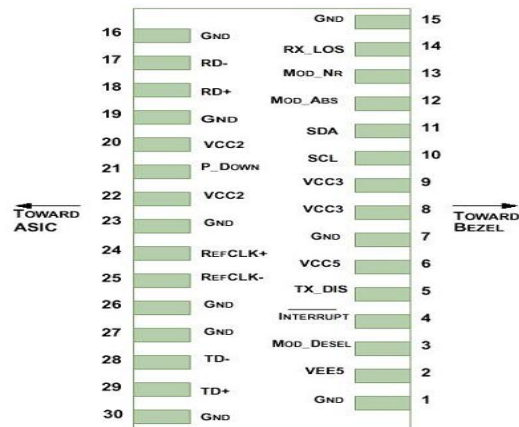
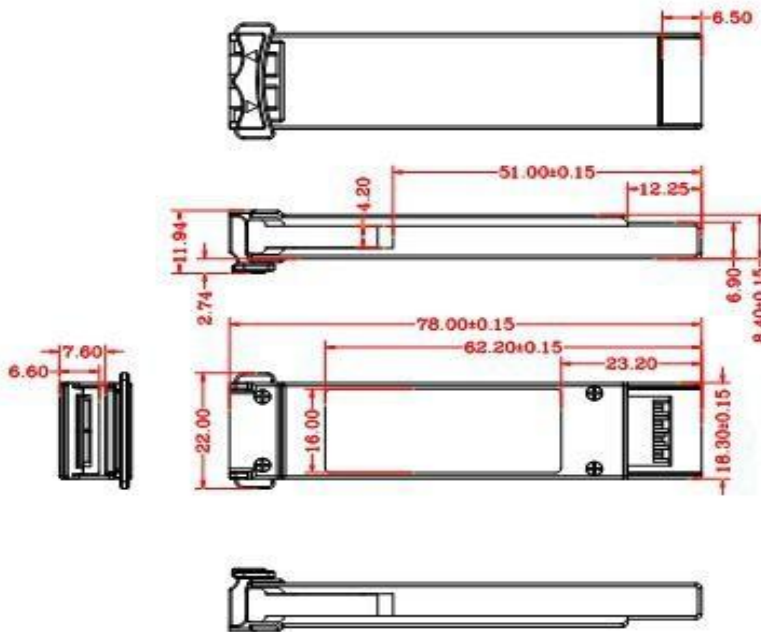


Diagram of Host Board Connector Block Pin Numbers and Name

■ Outline Dimensions (mm)



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